0410 2836 ~~0410~~ 0410

TSMC-00-004

September 5, 2000

#2 TQS L'Anderson 12-6-00

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/604,067 06/26/00

Ming-Dou Ker, Mau-Lin Wu

POWER-RAIL ESD CLAMP CIRCUITS WITH WELL-TRIGGERED PMOS

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,610,791 to Voldman, "Power Sequence Independent Electrostatic Discharge Protection Circuits", describes a power sequence independent electrostatic discharge protection circuits for multiple power supply busses of an integrated circuit.

The following articles describe ESD protection devices having uniform turn-on and current flow:

1) Stephen G. Beebe, "Methodology for Layout Design and Optimization of ESD Protection Transistors", 1996 EOS/ESD Symp. Proc., pp. 265-275.

2) Polgreen et al., "Improving the ESD Failure Threshold of Silicided n-MOS Output Transistors by Ensuring Uniform Current Flow", IEEE Trans. Electron Devices, Vol. 39, pp. 379-388, 1992.

3) Duvvury et al., "Dynamic Gate Coupling of NMOS for Efficient Output ESD Protection", Proc. of IRPS, 1992, pp. 141-150.

4) Duvvury et al., "Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability", Tech Dig. IEDM, 1992, pp. 131-134.

5) Ramaswamy et al., "EOS/ESD Reliability of Deep Sub-Micron NMOS Protection Devices", Proc. of IRPS, 1995, pp. 284-291.

6) Ker et al., "Capacitor-Couple ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS ASIC", IEEE Trans, on VLSI Systems, Vol. 4, pp. 307-321, September 1996.

7) Ming-Dou Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuits for Submicron CMOS VLSI", IEEE Trans. on Electron Devices, Vol. 46, No. 1, pp. 173-183, January 1999.

8) Merrill et al., "ESD Design Methodology", EOS/ESD Symp. Proc., 1994, EOS-16, pp. 141-149.

9) Dabral et al., "Core Clamps for Low Voltage Technologies", EPS/ESD Symp. Proc., 1994, EOS-16, pp.141-149.

10) Worley et al., "Sub-Micron Chip ESD Protection Schemes which Avoid Avalanching Junctions", EOS/ESD Symp. Proc., 1995, EOS-17, pp. 13-20.

11) Voldman et al., "Scaling, Optimization and Design Considerations of Electrostatic Discharge Protection Circuits in CMOS Technology", EOS/ESD Symp. Proc., pp. 251-260, 1993.

12) Amerasekera et al., "The Impact of Technology Scaling on ESD Robustness and Protection Circuit Design", EOS/ESD Symp. Proc., pp. 237-245, 1994.

13) Daniel et al., "Process and Design Optimization for Advanced CMOS I/O ESD Protection Devices", EOS/ESD Symp. Proc., pp. 206-213, 1990.

14) Chen et al., "Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes", Proc. of EOS/ESD Symp., pp. 230-239, 1997.

15) Amerasekera et al., "Substrate Triggering and Salicide Effects on ESD Performance and Protection Circuit Design in Deep Submicron CMOS Processes", IEDM Tech Digest. 1995, pp. 547-550.

16) Chen et al., "Design Methodology and Optimization of Gate-Driven NMOS ESD Protection Circuits in Submicron CMOS Processes", IEEE Trans. on Electron Devices, Vol. 45, No. 12, pp. 2448-2456, December 1998.

17) Anderson et al., "ESD Protection for Mixed-Voltage I/O Using NMOS Transistors Stacked in a Cascode Configuration", Proc. of EOS/ESD Symp., pp. 54-62, 1998.

U.S. Patent 5,631,793 to Ker et al., "Capacitor-Couple Electrostatic Discharge Protection Circuit", describes a capacitor-coupled electrostatic discharge protection circuit.

U.S. Patent 4,855,620 to Duvvury et al., "Output Buffer with Improved ESD Protection", describes an output buffer with ESD protection.

U.S. Patent 5,255,146 to Miller, "Electrostatic Discharge Detection and Clamp Control Circuit", describes an electrostatic discharge detection and clamp control circuit.

U.S. Patent 5,237,395 to Lee, "Power Rail ESD Protection Circuit", describes a power rail ESD protection circuit.

U.S. Patent 5,287,241 to Puar, "Shunt Circuit for Electrostatic Discharge Protection", describes a shunt circuit for electrostatic discharge protection between the power supply busses of an integrated circuit.

U.S. Patent 5,311,391 to Dungan et al., "Electrostatic Discharge Protection Circuit with Dynamic Triggering", describes an electrostatic discharge protection circuit with dynamic triggering.

U.S. Patent 5,440,162 to Worley et al., "ESD Protection for Submicron CMOS Circuits", describes an ESD protection for submicron CMOS circuits.

U.S. Patent 5,625,280 to Voldman, "Voltage Regulator Bypass Circuit", describes a voltage regulator bypass circuit to protect a voltage regulator during an ESD event.

U.S. Patent 5,086,365 to Lien, "Electostatic Discharge Protection Cirtuit", describes an electostatic discharge protection circuit.

Sincerely,

George O. Saile

George O. Saile, Reg. No. 19572